REMARKS

The Office Action mailed February 6, 2008 has been received and carefully noted. Claims 1-27 are currently pending in the subject application and are presently under consideration.

Claims 1, 2, and 23 have been amended herein without adding new matter. Support for the amendments can be found in at least pg. 11 of the Specification. Thus, entry thereof is respectfully requested. A listing of claims can be found on pages 2-7 of this Reply.

Favorable reconsideration of the pending claims is respectfully requested in view of the amendments and the following comments.

I. Rejection of Claim 1 Under 35 U.S.C. § 102(e)

Claim 1 stands rejected under 35 U.S.C. §102(e) as anticipated by Andrews *et al.* (U.S. 2005/0122339). This rejection should be withdrawn for at least the following reason. Andrews *et al.* does not expressly or inherently describe each and every aspect of the claim.

Amended tndependent claim 1 recites: "a render-cache controller to ***maintain the order in which each thread*** is dispatched to the graphics engine in line with the multithreading, multi-core graphics engine processing the pixel data corresponding to each thread" (emphasis added). The Examiner cites Andrews *et al.* at paragraph 0066 as relating to this aspect (*See* Office Action mailed February 6, 2008, pgs. 2-3). The Applicants respectfully disagree. At paragraph 0066, Andrews *et al.* discloses differentiating between threads that may access only unlocked sets of a cache and threads that may access both locked sets and unlocked sets of the cache. However, Andrews *et al.* is silent with respect to "a render-cache controller to maintain the order in which ***each thread*** is dispatched to the graphics engine in line with the multithreading, multi-core graphics engine processing the pixel data corresponding to

each thread" (emphasis added). The cited reference fails to disclose any dispatching order of individual threads.

In view of the foregoing, it is readily apparent that Andrews *et al.* does not describe each and every element of independent claim 1. Accordingly, it is respectfully requested that this rejection be withdrawn.

II. Rejection of Claims 2, 3, 5, and 23-25 Under 35 U.S.C. § 103(a)

Claims 2, 3, 5, and 23-25 stand rejected under 35 U.S.C. § 103(a) as being obvious over Andrews *et al.*, in view of Chrysos *et al.* (U.S. 6,549,930). It is respectfully requested that these rejections be withdrawn for at least the following reason. Andrews *et al.* and Chrysos *et al.*, alone or in combination, do not teach or suggest all the limitations of these claims.

Amended independent claim 23 recites: "a render-cache controller to maintain the order in which ***each thread*** is dispatched to the graphics engine in line with the multithreading, multi-core graphics engine processing the pixel data corresponding to each thread" (emphasis added). For the reasons described above, Andrews *et al.* does not disclose this aspect. The Examiner does not indicate and the Applicants do not discern any part of Chrysos *et al.* that cures the aforementioned deficiencies of Andrews *et al.* regarding this claim. Thus, Andrews *et al.* and Chrysos *et al.*, alone or in combination, fail to teach or suggest this aspect of amended independent claim 23.

Amended independent claim 23 also recites: "the render-cache controller having a pixel mask array to identify in flight pixel data, the render-cache controller having a cache-line status array to identify availability of a cache-line in the render-cache." The Examiner has not indicated and the Applicants do not discern any part of Andrews *et al.* and Chrysos *et al.* that discloses these aspects.

Each of the dependent claims depends from one of independent claims 1 and 23. For the same reasons regarding the independent claims, Andrews *et al.* and Chrysos *et al.* do not teach or suggest all the limitations of these dependent claims. Reconsideration and withdrawal of these rejections are respectfully requested.

III. Rejection of Claims 4, 6-10, 26, and 27 Under 35 U.S.C. § 103(a)

Claims 4, 6-10, 26, and 27 stand rejected under 35 U.S.C. § 103(a) as being obvious over Andrews *et al.*, Chrysos *et al.*, and Hussain (U.S. 2004/0233208). Each of these dependent claims depends from one of independent claims 1 and 23. The Examiner does not indicate and the Applicants do not discern any part of Hussain that cures the aforementioned deficiencies of Andrews *et al.* and Chrysos *et al.* regarding the independent claims. For the same reasons regarding the independent claims, Andrews *et al.*, Chrysos *et al.*, and Hussain do not teach or suggest all the limitations of these dependent claims. Reconsideration and withdrawal of these rejections are respectfully requested.

IV. Rejection of Claims 11-13, 15-20, and 22 Under 35 U.S.C. § 103(a)

Claims 11-13, 15-20, and 22 stand rejected under 35 U.S.C. § 103(a) as being obvious over Hussain, in view of Chrysos *et al.* It is respectfully requested that these rejections be withdrawn for at least the following reason. Hussain and Chrysos *et al.*, alone or in combination, do not teach or suggest all the limitations of these claims.

Independent claim 11 recites:

> a pixel mask array having a mask bit for every entry of the content addressable memory, each mask bit to indicate whether previously allocated pixel data is in flight; and,
> a cache-line status array with a status bit for every entry of the content addressable memory, each status bit to indicate the availability of a cache-line in the render-cache.

The Examiner contends that Hussain teaches the pixel mask array at paragraph 0043 and teaches the cache-line status array at paragraphs 0044-0046 (*See* Office Action mailed February 6, 2008, pg. 12). In addition, the Examiner concedes that Hussain does not disclose "each mask bit to indicate whether previously allocated pixel data is in flight," but contends that Chrysos *et al.* discloses "indicating that pixel data is in flight" at Figure 5, element 505 (*See* Office Action mailed February 6, 2008, pg. 12).

However, neither of the cited references teaches each mask bit in a pixel mask array to indicate whether previously allocated pixel data is in flight. Paragraphs 0043-0046 of Hussain disclose the manner in which a pixel cache is used to handle requests for pixels from a graphics pipeline. After the request is received, a tag compare is performed to determine whether the requested pixel data is in the pixel cache (*See* Hussain, paragraph 0043). If so, then the requested data is retrieved from the cache (*See Id.*). If not, then a search is performed to determine whether a cache line in the pixel cache is free (*See* Hussain, paragraph 0044). If no cache lines are free, then the process waits for a free cache line (*See* Hussain, paragraph 0045). If a cache line becomes free, then the process determines whether that free cache line is dirty. A cache line is dirty when at least one sub-block in the cache line has been updated, but the change to the sub-block has not yet been written to main memory (*See* Hussain, paragraph 0046). If the free cache line is not dirty, then a "read request is issued for the uncached data to be retrieved from memory into the selected cache line" (*See* Hussain, paragraph 0047). If the free cache line is dirty, then both a read request and a write request are issued because in addition to the read request described above, a write request writes back to memory the content of the dirty cache line (*See* Hussain, paragraph 0048).

First, Hussain's "pixel cache" does not teach "a pixel mask array having a mask bit for ***every entry*** of the content addressable memory" and "a cache-line status array with a status bit for ***every entry*** of the content addressable memory" (emphasis added). The pixel cache contains pixel data, but the reference is silent regarding the pixel cache containing a both mask bit **and** a status bit "for ***every entry*** of the content addressable memory" (emphasis added).

Second, Hussain and Chrysos *et al.* do not disclose "each mask bit to indicate whether previously allocated pixel data is in flight." The Examiner contends that Hussain discloses a "mask bit," but concedes that Hussain does not disclose "indicating that pixel data is in flight" (*See* Office Action mailed February 6, 2008, pg. 12). The Examiner thus relies on Chrysos *et al.* at Figure 5, element 505 for "indicating that pixel data is in flight" (*See* Office Action mailed February 6, 2008, pg. 12). However, citing Hussain for the "mask bit" and Chrysos *et al.* for "indicating that pixel data is in flight"

is not appropriate. The claim recites that each mask bit indicates whether previously allocated pixel data is in flight, and if Hussain teaches the mask bit, then Hussain ought to teach the recited characteristics of this mask bit (*i.e.*, that the mask bit indicates whether previously allocated pixel data is in flight). Chrysos *et al.* at Figure 5, element 505 discloses a filter for filtering instructions. This filter is not directed to mask bits of a pixel mask array, much less mask bits to indicate whether previously allocated pixel data is in flight. If the Examiner maintains these rejections, the Applicants respectfully request that the Examiner clarify and particularly point out the elements of Hussain or Chrysos *et al.* that teach a pixel mask array having a mask bit for every entry of the content addressable memory, the mask bits that indicate whether previously allocated pixel data is in flight, a cache-line status array with a status bit for every entry of the content addressable memory, and the status bits that indicate the availability of a cache-line in the render-cache.

Independent claim 18 recites:

> if the pixel data for the particular pixel has been previously allocated to the render-cache then
> ***checking the pixel mask array to determine whether the previously allocated pixel data is in flight***,
> stalling, if the previously allocated pixel data is in flight, and
> dispatching a thread to the graphics engine if the previously allocated pixel data is not in-flight

(emphasis added). The Examiner concedes that Hussain does not disclose these aspects, but contends that Chrysos *et al.* discloses these aspects at col. 14, line 53 – col. 15, line 3 and col. 26, line 54 – col. 27, line 20 (*See* Office Action mailed February 6, 2008, pg. 15).

The first cited passage of Chrysos *et al.* (col. 14, line 53 – col. 15, line 3) discloses an instruction of a processor that includes a "sample bit" that indicates that the instruction is in flight, but does not disclose a pixel mask array. The "sample bit" indicates in flight status, which begins at the time the instruction is fetched until the

instruction retires or is aborted. However, this "sample bit" is not in a pixel mask array, but rather is in an instruction of a processor. Chrysos *et al.* is silent regarding a pixel mask array and therefore does not teach "checking the pixel mask array to determine ***whether the previously allocated pixel data is in flight***."

The second cited passage of Chrysos *et al.* (col. 26, line 54 – col. 27, line 20) discloses scheduling of threads in a multithreaded processor according to processor utilization, but also does not disclose the pixel mask array. Chrysos *et al.* discloses scheduling the threads such that the utilization of the threads is non-conflicting. There is no indication of a pixel mask array to determine whether the previously allocated pixel data is in flight. If the Examiner maintains these rejections, the Applicants respectfully request that the Examiner clarify which particular element of Chrysos *et al.* discloses the pixel mask array that determines whether the previously allocated pixel data is in flight.

Each of the dependent claims depends from one of independent claims 11 and 18. For the same reasons regarding the independent claims, Hussain and Chrysos *et al.* do not teach or suggest all the limitations of these dependent claims. Reconsideration and withdrawal of these rejections are respectfully requested.

V. Rejection of Claim 14 Under 35 U.S.C. § 103(a)

Claim 14 stands rejected under 35 U.S.C. § 103(a) as being obvious over Hussain, in view of Chrysos *et al.*, and further in view of Baylor *et al.* (U.S. 2002/0078124). This claim depends from independent claim 11. The Examiner does not indicate and the Applicants do not discern any part of Baylor *et al.* that cures the aforementioned deficiencies of Hussain and Chrysos *et al.* Thus, for at least the reasons mentioned above regarding independent claim 11, the cited references do not teach or suggest all the limitations of claim 14. Withdrawal of this rejection is respectfully requested.

VI. Rejection of Claim 21 Under 35 U.S.C. § 103(a)

Claim 21 is rejected under 35 U.S.C. 103(a) as being obvious over Hussain, in view of Chrysos *et al.*, and further in view of Andrews *et al.*. Claim 21 depends from independent claim 18. The Examiner does not indicate and the Applicants do not discern any part of Andrews *et al.* that cures the aforementioned deficiencies of Hussain and Chrysos *et al.* Thus, for at least the reasons mentioned above regarding independent claim 18, the cited references do not teach or suggest all the limitations of claim 18. Withdrawal of this rejection is respectfully requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,
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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being submitted to the United States Patent and Trademark Office electronically via EFS Web on the date shown below.

Robert Fiore — 5/6/08 Date